Abstract

A processor having a packet processing order maintenance feature includes classification circuitry operative to identify for each of a plurality of packets received in the processor a corresponding packet flow identifier, control circuitry operatively coupled to the classification circuitry, and at least one operational unit operatively coupled to the control circuitry. The control circuitry is operative to direct one or more packets having a given packet flow identifier to the operational unit(s) in a manner that maintains a desired function call sequencing over the one or more packets having the given packet flow identifier for one or more order-dependent processing tasks in the processor.